In the Claims:

1. (Currently Amended) ~~An apparatus~~ A memory controller, comprising:

an array of tag address storage locations; and

a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache ~~associated with~~ located on a memory module, the command sequencer and serializer unit to control the data cache ~~associated with~~ located on the memory module by delivering a plurality of commands over a plurality of command and address lines, the commands delivered over a plurality of transfer periods, the plurality of commands including an activate command and a cache fetch command, the activate and cache fetch commands differing in format only in the information delivered during a last transfer period.

A1

2. (Currently Amended) ~~The apparatus~~ The memory controller of claim 1, the activate command and the cache fetch command differing in cache hit information delivered during the last transfer period.

3. (Currently Amended) ~~The apparatus~~ The memory controller of claim 2, the cache fetch command further including way information delivered during the last transfer period.

4. (Currently Amended) ~~The apparatus~~ The memory controller of claim 3, the plurality of commands each delivered over four transfer periods.

5. (Currently Amended) ~~The apparatus~~ The memory controller of claim 4, the activate and cache fetch commands each including memory module destination information during a first transfer period.

6. (Currently Amended) ~~The apparatus~~ The memory controller of claim 5, the activate and cache fetch commands each including row address information during each of the four transfer periods.

A1

7. (Currently Amended) ~~The apparatus~~ The memory controller of claim 1, the plurality of commands further including a read command and a read and preload command, the read and read and preload commands differing in format only in the information delivered during a last transfer period.

8. (Currently Amended) ~~The apparatus~~ The memory controller of claim 7, the read command and read and preload command differing in cache hit information delivered during the last transfer period.

9. (Currently Amended) ~~The apparatus~~ The memory controller of claim 8, the read and preload command further including way information delivered during the last transfer period.

10. (Currently Amended) ~~The apparatus~~ The memory controller of claim 9, the plurality of commands each delivered over four transfer periods.

11. (Currently Amended) ~~The apparatus~~ The memory controller of claim 10, the read command and the read and preload command each including memory module destination information during a first transfer period.

12. (Currently Amended) ~~The apparatus~~ The memory controller of claim 11, the read command and read and preload command each including column address information during each of the four transfer periods.

13. (Currently Amended) A memory module ~~An apparatus~~, comprising:

at least one memory device; and

a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by a memory controller component over a memory bus, the memory controller component including an array of tag address storage locations, the commands delivered over a plurality of transfer periods, the plurality of commands including an activate command and a cache fetch command, the activate and cache fetch commands differing in format only in the information delivered during a last transfer period.

14. (Currently Amended) The memory module ~~The apparatus~~ of claim 13, the activate command and the cache fetch command differing in cache hit information delivered during the last transfer period.

15. (Currently Amended) The memory module ~~The apparatus~~ of claim 14, the cache fetch command further including way information delivered during the last transfer period.

16. (Currently Amended) The memory module ~~The apparatus~~ of claim 15, the plurality of commands each delivered over four transfer periods.

A1

17. (Currently Amended) The memory module ~~The apparatus~~ of claim 16, the activate and cache fetch commands each including memory module destination information during a first transfer period.

18. (Currently Amended) The memory module ~~The apparatus~~ of claim 17, the activate and cache fetch commands each including row address information during each of the four transfer periods.

19. (Currently Amended) A system, comprising:

a processor;

a memory controller coupled to the processor, the memory controller including

an array of tag address storage locations, and

a command sequencer and serializer unit coupled to the array of tag address storage locations; and

a memory module coupled to the memory controller via a memory bus, the memory module including

at least one memory device, and

a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, the commands delivered over a plurality of transfer periods, the plurality of commands including an activate command and a cache fetch command, the activate and cache fetch commands differing in format only in the information delivered during a last transfer period.

A1

20. (Original) The system of claim 19, the activate command and the cache fetch command differing in cache hit information delivered during the last transfer period.

21. (Original) The system of claim 20, the cache fetch command further including way information delivered during the last transfer period.

22. (Original) The system of claim 21, the plurality of commands each delivered over four transfer periods.

23. (Original) The system of claim 22, the activate and cache fetch commands each including memory module destination information during a first transfer period.

24. (Original) The system of claim 23, the activate and cache fetch commands each including row address information during each of the four transfer periods.

25. (Currently Amended) A method, comprising:

delivering during a first plurality of transfer periods information corresponding to both an activate command and a cache fetch command from a memory controller to a memory module over a memory bus; and

delivering from the memory controller to the memory module during a last transfer period information differentiating between an activate command and a cache fetch command.

A1

26. (Original) The method of claim 25, wherein delivering during a last transfer period information differentiating between an activate command and a cache fetch command includes delivering cache hit information.

27. (Currently Amended) A method, comprising:

delivering during a first plurality of transfer periods information corresponding to both a read command and a read and preload command from a memory controller to a memory module over a memory bus; and

delivering from the memory controller to the memory module during a last transfer period information differentiating between a read command and a read and preload command.

28. (Original) The method of claim 27, wherein delivering during a last transfer period information differentiating between a read command and a read and preload command includes delivering cache hit information.